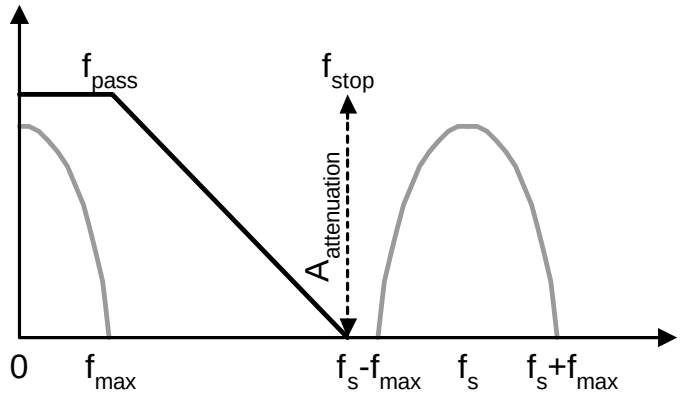
Discrete-Time Filter
(Switched-Capacitor Filter)

Discrete-Time Filters

- **Anti-Aliasing Filter & Smoothing Filter**

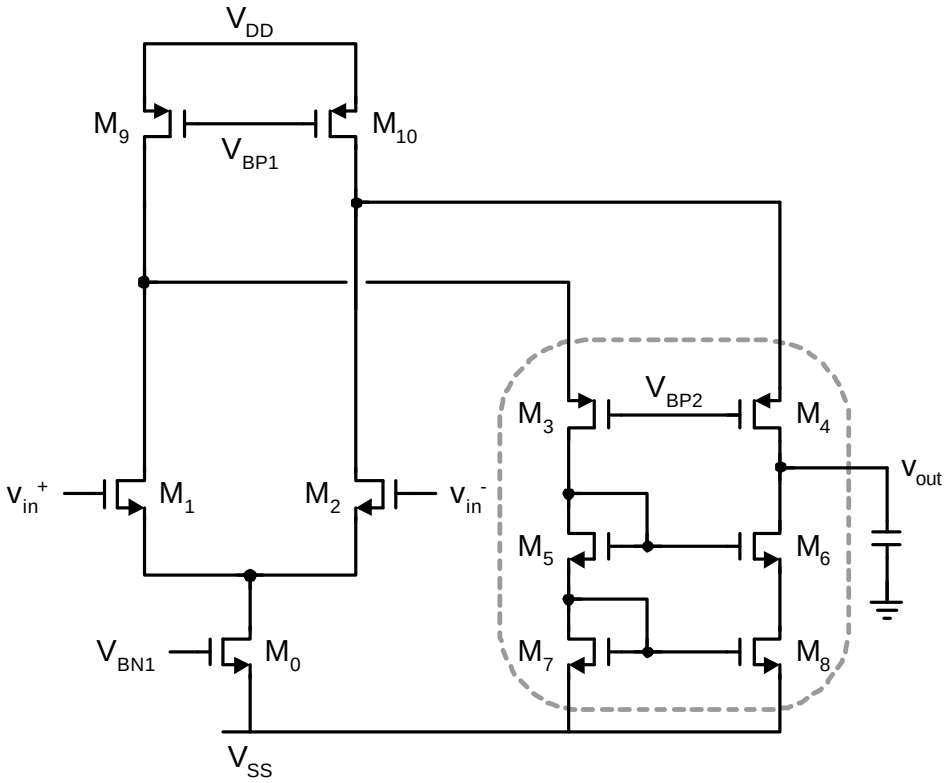


- **FIR Filters**
  - ➔ Windowing (Kaiser), Optimization
- **IIR Filters**
  - ➔ Frequency Transformation from C-T Filters
  - ➔ Forward / Backward Euler Transformation
  - ➔ Bilinear Transformation
  - ➔ Lossless Discrete Integrator (LDI) Transformation

SC Circuit Motivation

- **Active RC Filter**
  - ➔ RC Time-Constant Variation ~ 30%
  - ➔ Capacitance Ratio Variation ~ 0.1%
- **Building Blocks Well Integrated**
  - ➔ Operational Amplifier : Folded-Cascode Configuration
  - ➔ Capacitor : Poly1-Poly2, Metal-Metal
  - ➔ Switches : Transmission Gate
  - ➔ Multi-Phase Non-Overlapping Clocks

Folded-Cascode Op Amp



- Single-Stage Op Amp
- Frequency Compensation
  by Load Capacitance C_L
- DC voltage gain

$$A_V(0) = g_{m1} \cdot R_{out} \approx g_{m1} \cdot \left[g_m r_{ds}^{\,2} \right]$$

- Unity-Gain Frequency

$$\omega_{0dB} = g_{m1}/C_L$$

- Slew Rate

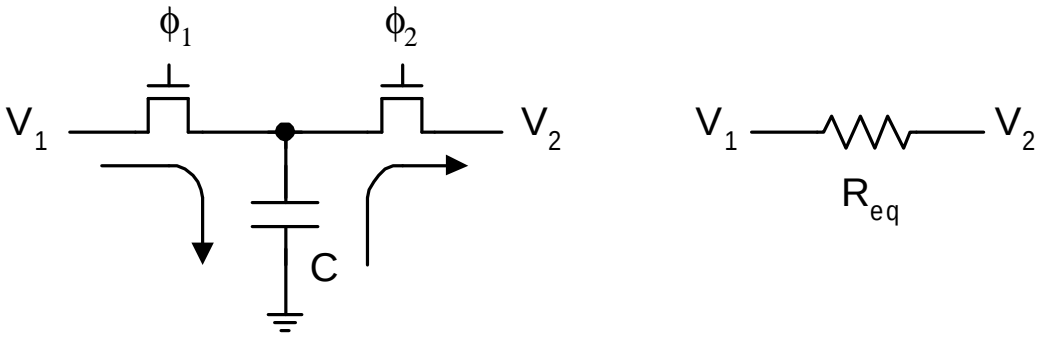
$$SR = I_0/C_L$$

- **Fully Differential Version**

SC Circuit Applications

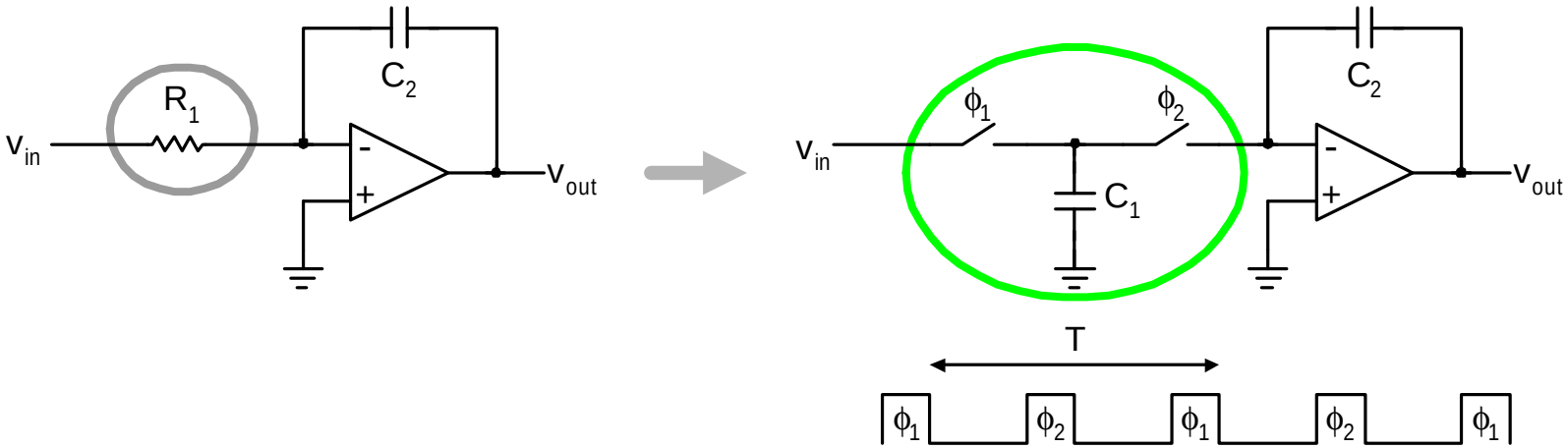
- **Analog Discrete-Time Filters**
- **Analog Discrete-Time Signal Processing Circuits**
  - ➔ Voltage Amplifiers, VGA
  - ➔ Interpolators, Decimations
  - ➔ Modulators, Demodulators, Mixers
  - ➔ Oscillators, Waveform Generators, ……
- **Data Transceivers : Telecom IC, CODEC, Baseband Processors, ….**
- **Data Converters**
  - ➔ DAC : Charge-Redistribution, Cyclic (Algorithmic)
  - ➔ ADC : Successive Approximation, Cyclic (Algorithmic), Pipeline
  - ➔ Sigma-Delta Modulators
- **Other Areas**

Basic Idea of SC Circuits



- Charge Transfer ($V_1 \Rightarrow V_2$) $\Delta Q = Q_1 - Q_2 = C \cdot (V_1 - V_2)$
- Average Current during T $I_{avg} \equiv \frac{\Delta Q}{T} = \frac{C \cdot (V_1 - V_2)}{T}$
- Equivalent Resistance $R_{eq} \equiv \frac{V_1 - V_2}{I_{avg}} = \frac{C}{T} = \frac{1}{C f_S}$

RC vs SC Integrators



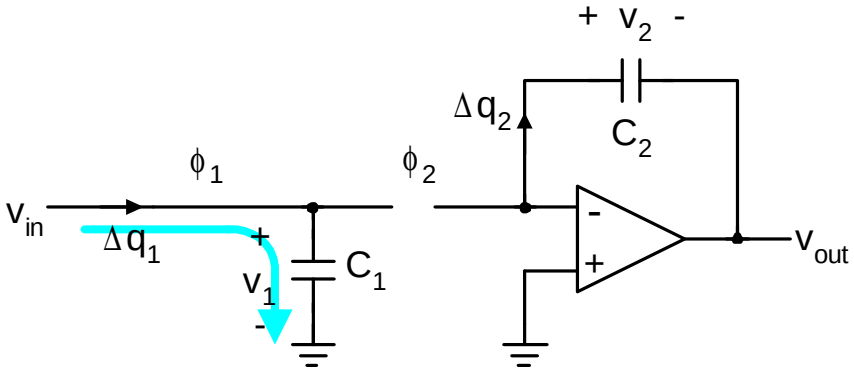
- **Passive Resistor ➔ Switched-Capacitor Branch**

$$v_{out}(t) = -\frac{1}{R_1 C_2}\int_{-\infty}^{t} v_{in}(\tau)\,d\tau \Rightarrow \; H_a(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{R_1 C_2}\cdot\frac{1}{s}$$

- **Requirements**

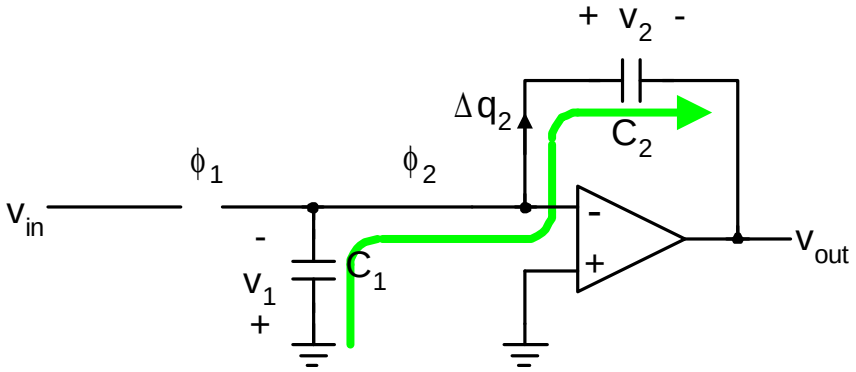
$$C_1 = \frac{T}{R_1}$$

SC Integrator Operations



- $f_1 = 1$

$$q_1(n) = C_1 \cdot v_1(n) = C_1 \cdot v_{in}(n)$$
$$q_2(n) = C_2 \cdot v_2(n) = C_2 \cdot [0 - v_{out}(n)]$$



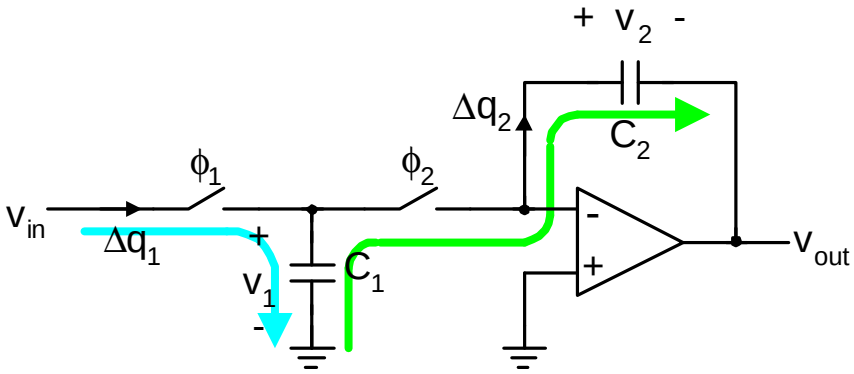
- $f_2 = 1$

$$q_1(n) = C_1 \cdot v_1(n) = C_1 \cdot 0$$
$$q_2(n) = C_2 \cdot v_2(n) = C_2 \cdot [0 - v_{out}(n)]$$

- **at the integration time (f_2=1) → n, (f_1=1) → n-1, $Dq_1 = Dq_2$**

$$\Delta q_1(n) = q_1(n) - q_1(n-1) = 0 - \{-C_1 \cdot v_{in}(n-1)\}$$
$$\Delta q_1(n) = q_2(n) - q_2(n-1) = C_2 \cdot [0 - v_{out}(n)] - C_2 \cdot [0 - v_{out}(n-1)]$$
$$\therefore C_2 \cdot [v_{out}(n) - v_{out}(n-1)] = -C_1 \cdot v_{in}(n-1)$$

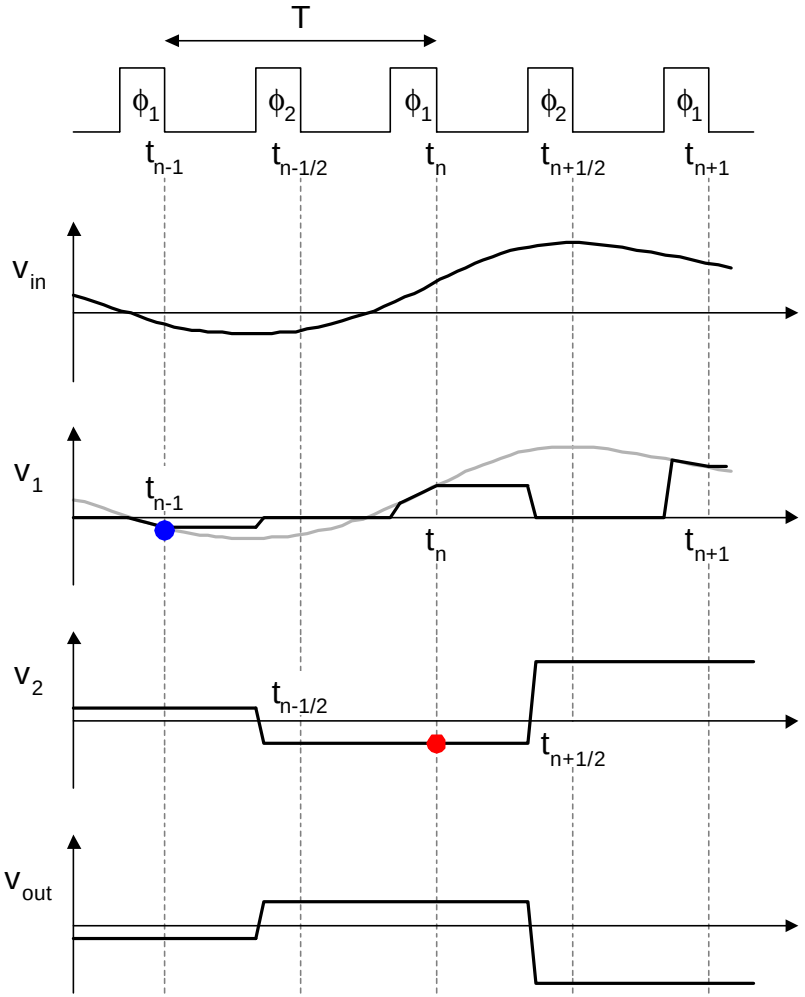
Basic SC Integrator 1



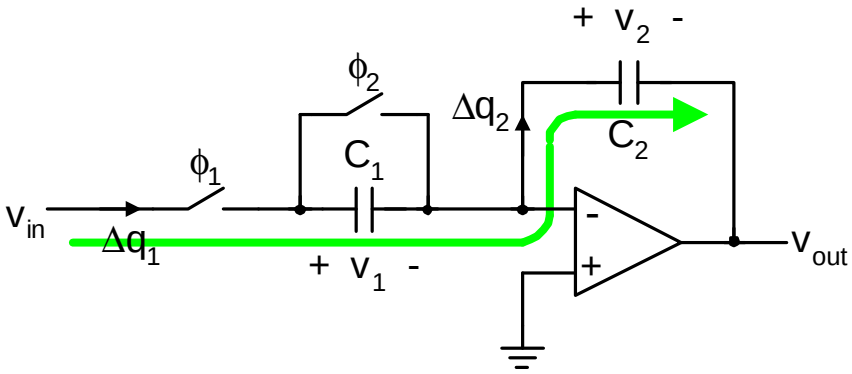
$$\Delta q_1 = C_1 \cdot [0 - \{- v_{in}(n-1)\}]$$
$$\Delta q_2 = C_2 \cdot [v_2(n) - v_2(n-1)]$$
$$= -C_2 \cdot [v_{out}(n) - v_{out}(n-1)]$$

$$C_1 \cdot z^{-1} V_{in}(z) = -C_2 \cdot [1 - z^{-1}] \cdot V_{out}(z)$$

$$\therefore H(z) \equiv \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}}$$



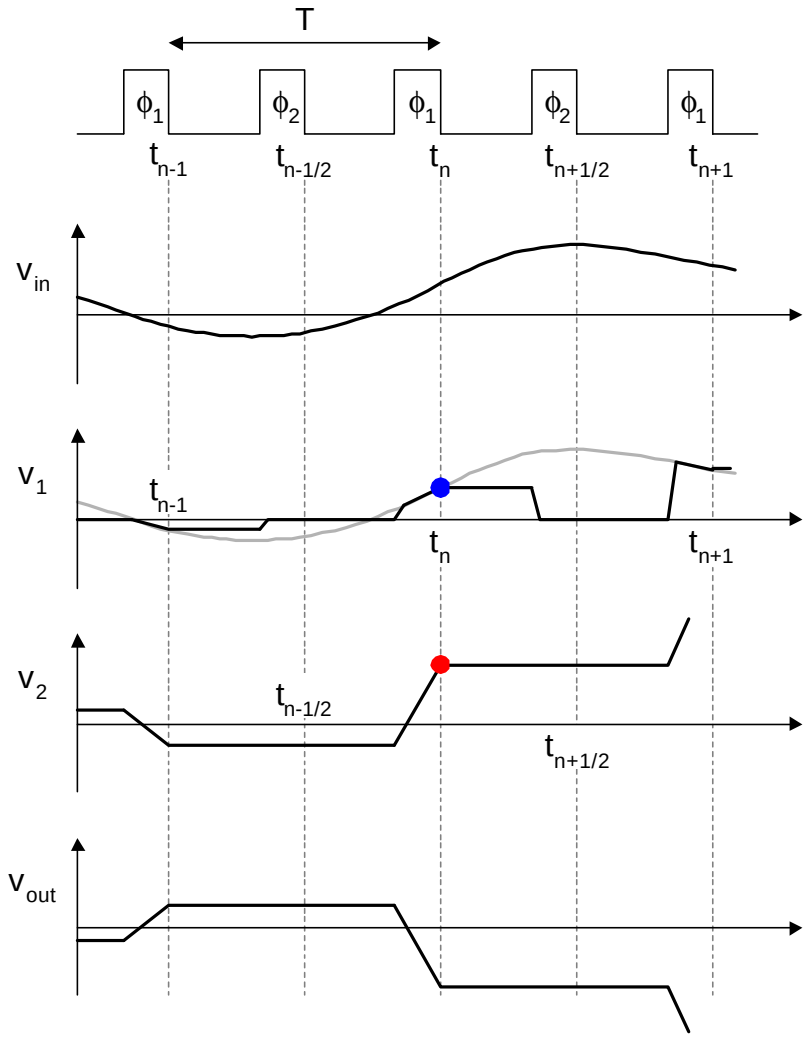
Basic Integrator 2



$$\Delta q_1 = C_1 \cdot [v_{in}(n) - 0]$$
$$\Delta q_2 = C_2 \cdot [v_2(n) - v_2(n-1)]$$
$$= -C_2 \cdot [v_{out}(n) - v_{out}(n-1)]$$

$$C_1 \cdot V_{in}(z) = -C_2 \cdot [1 - z^{-1}] \cdot V_{out}(z)$$

$$\therefore H(z) \equiv \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2} \cdot \frac{1}{1 - z^{-1}}$$



Frequency Response of SCI

- Transfer Function

$$H\left(e^{j\Omega T}\right) \equiv H(z)\Big|_{z=e^{j\Omega T}} = -\frac{C_1}{C_2}\cdot\frac{1}{e^{j\Omega T}-1}$$

- Condition : $\Omega T << 1$

$$H\left(e^{j\Omega T}\right) \cong -\frac{C_1}{C_2}\cdot\frac{1}{\left(1+j\Omega T-\frac{1}{2}(\Omega T)^2-\cdots\right)-1} \cong -\frac{C_1}{C_2}\cdot\frac{1}{j\Omega T}$$

- Continuous-Time Integrator

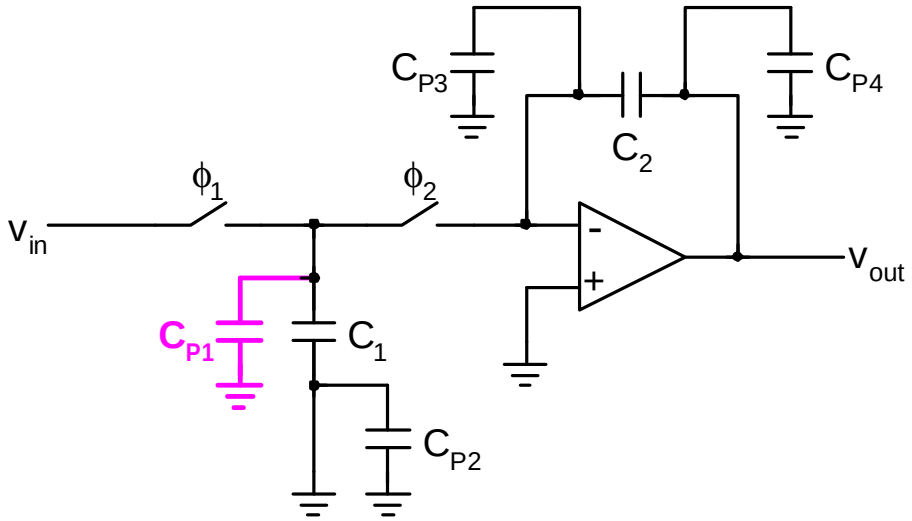
$$H(j\Omega) \equiv H(s)\Big|_{s=j\Omega} = -\frac{1}{R_1 C_2}\cdot\frac{1}{j\Omega}$$

- For Same Frequency Response

$$C_1 = \frac{T}{R_1}$$

C_1/C_2 & T accurate

Parasitic Capacitance Problem



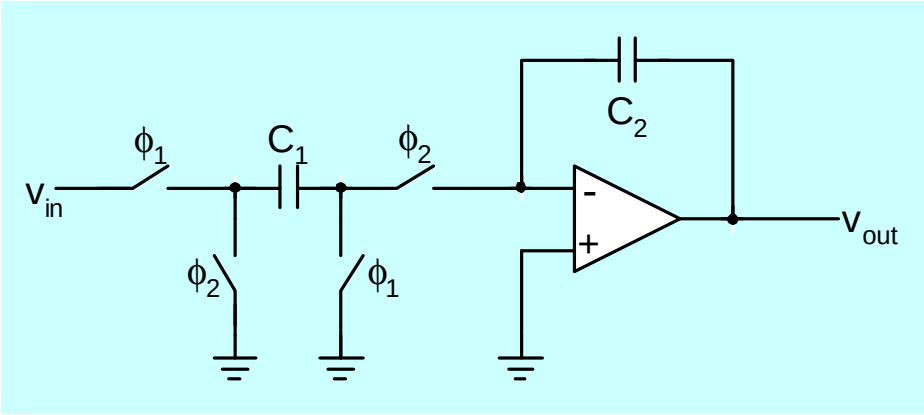
✓ C_{P1} ➔ $H(z) = -\frac{C_1 + \mathbf{C_{P1}}}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}}$

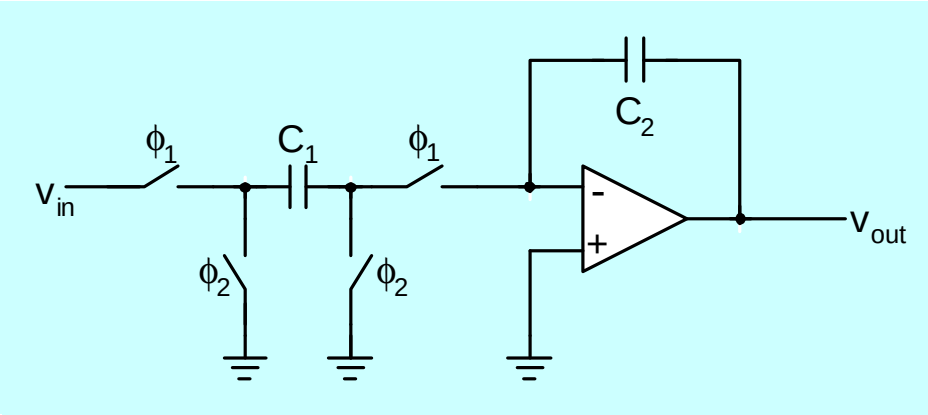
✓ C_{P2} : Connected to GND

✓ C_{P3} : Connected to Virtual GND

✓ C_{P4} : Connected to Output of an Amplifier

Parasitic-Insensitive SC Integrators





$$H(z) \equiv \frac{V_{out}(z)}{V_{in}(z)} = +\frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}}$$

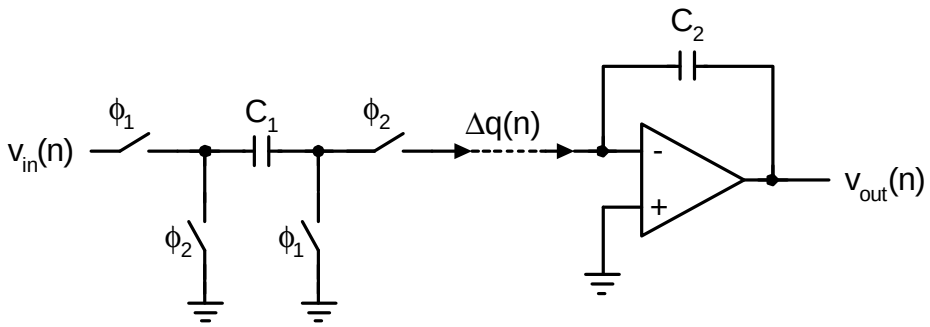
$$H(z) \equiv \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2} \cdot \frac{1}{1 - z^{-1}}$$

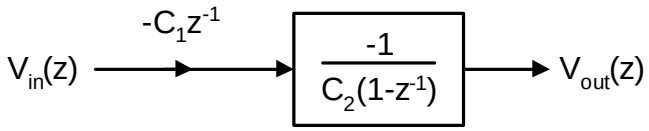
All Parasitic Capacitors Connected to

➔ GND / Virtual GND

➔ Voltage Source / Output of Amplifier

Signal Flow Graph Establishment





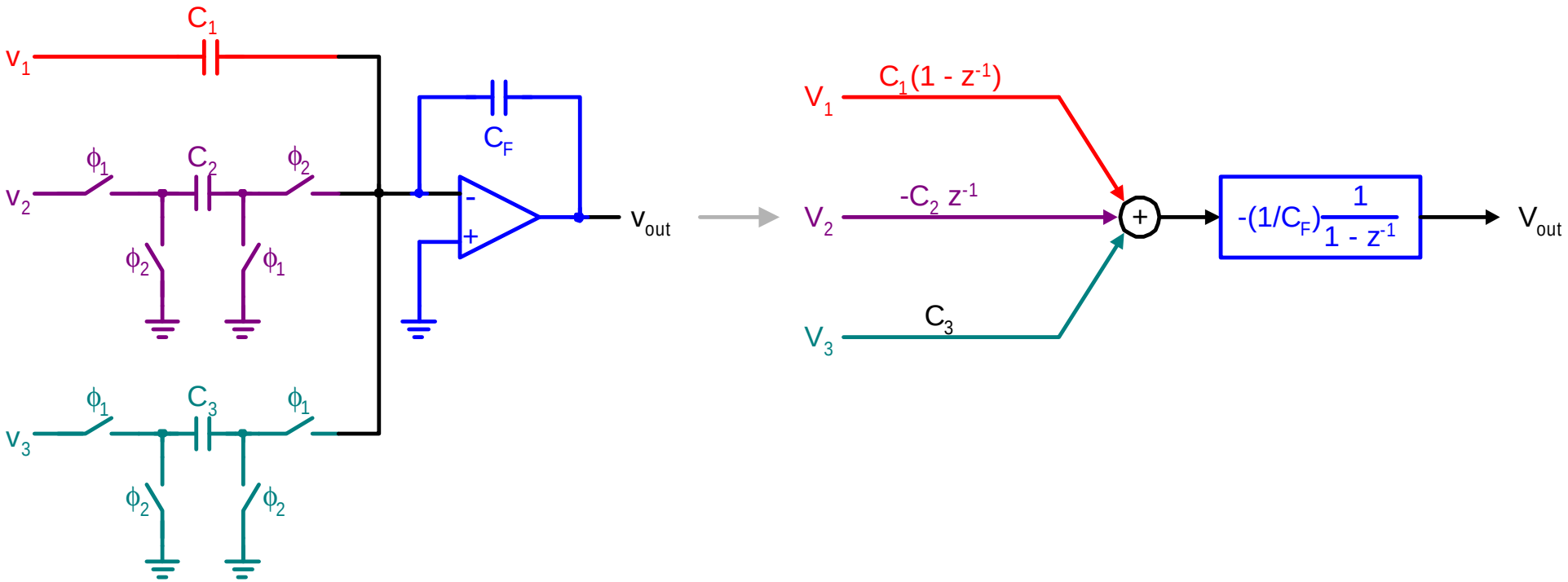
- **Switched-C_1 Branch ➔ Input : $V_{in}(z)$, Output : $\Delta Q(z)$**

$$\Delta q(n) = q(n) - q(n-1) = C_1 \cdot [0 - v_{in}(n)]$$
$$\Delta Q(z) = -C_1 \cdot z^{-1} \cdot V_{in}(z)$$

- **Op Amp w/ Feedback C_2 ➔ Input : $\Delta Q(z)$, Output : $V_{out}(z)$,**

$$v_{out}(n) - v_{out}(n-1) = -\Delta q(n)/C_2$$
$$V_{out}(z) = -\frac{1}{C_2 \cdot (1 - z^{-1})} \cdot \Delta Q(z)$$

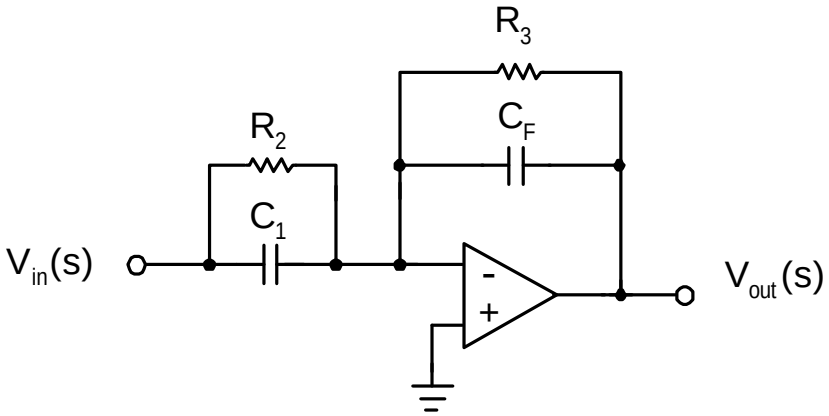
Signal Flow Graph for SC Integrators



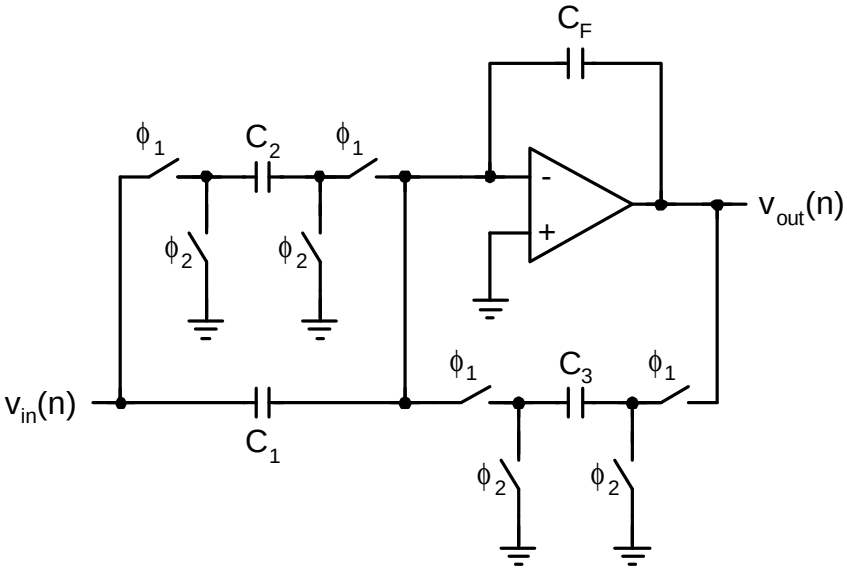
$$V_{out}(z) = -\frac{C_1}{C_F} \cdot V_1(z) + \frac{C_2}{C_F} \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot V_2(z) - \frac{C_3}{C_F} \cdot \frac{1}{1 - z^{-1}} \cdot V_3(z)$$

1st-Order SC Filter

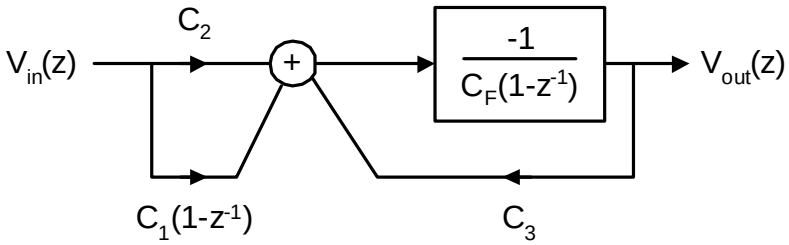
- **Active RC Version**



- **SC Version**



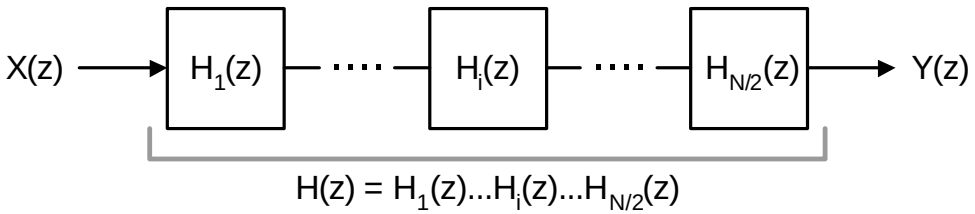
- **Signal Flow Graph**



$$H(z) \equiv \frac{V_{out}(z)}{V_{in}(z)} = -\frac{\frac{C_1 + C_2}{C_F} - \frac{C_1}{C_F} z^{-1}}{1 + \frac{C_3}{C_F} - z^{-1}}$$

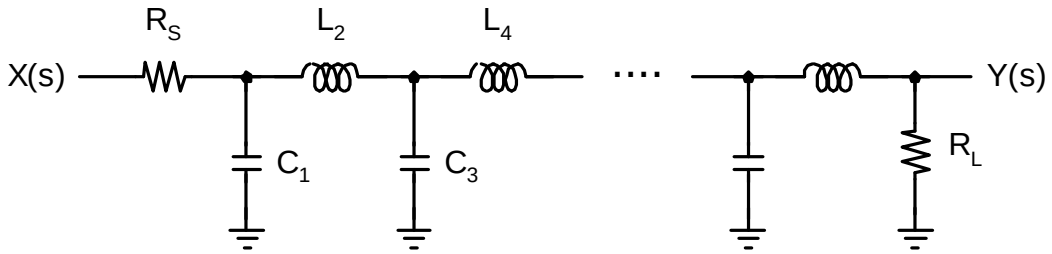
High-Order Filter Implementation

- **Cascade of Biquad Blocks**



$$H(z)=\prod_{i=1}^{N/2}H_i(z)=\prod_{i=1}^{N/2}\frac{b_2z^2+b_1z+b_0}{a_2z^2+a_1z+a_0}$$

- **RLC Prototype**

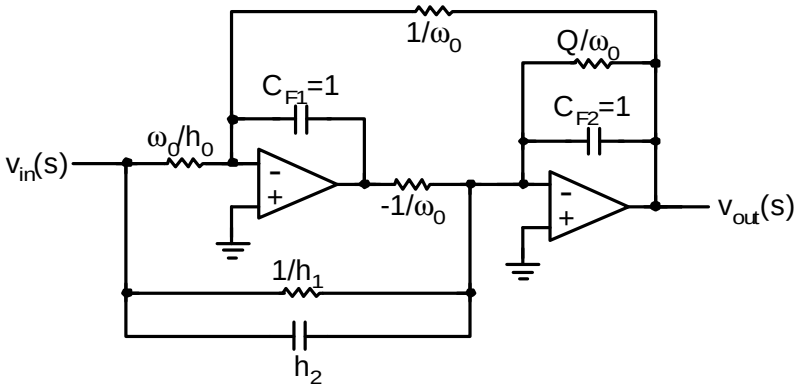


$$I_2(s)=\frac{1}{sL_2}\cdot[V_1(s)-V_2(s)]$$

$$I_2(z)=I_2(s)\Big|_{s=\frac{2}{T}\frac{z-1}{z+1}}$$

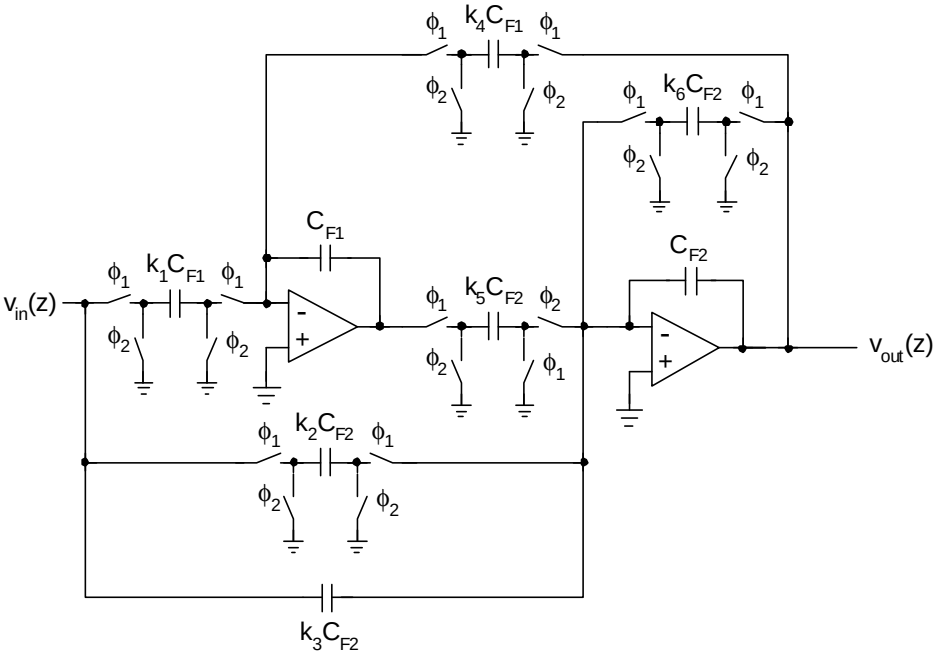
Low-Q SC Biquad

- **Active RC Version**



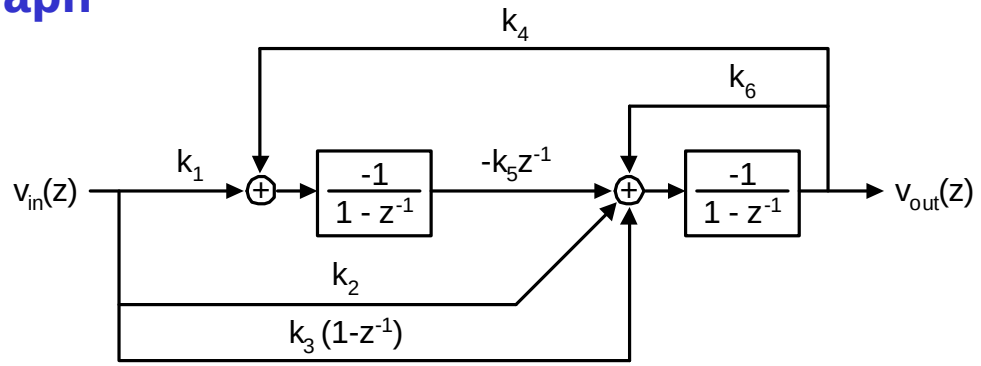
$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = -\frac{h_2 s^2 + h_1 s + h_0}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2}$$

- **SC Version**



Low-Q SC Biquad (cont'd)

- **Signal Flow Graph**



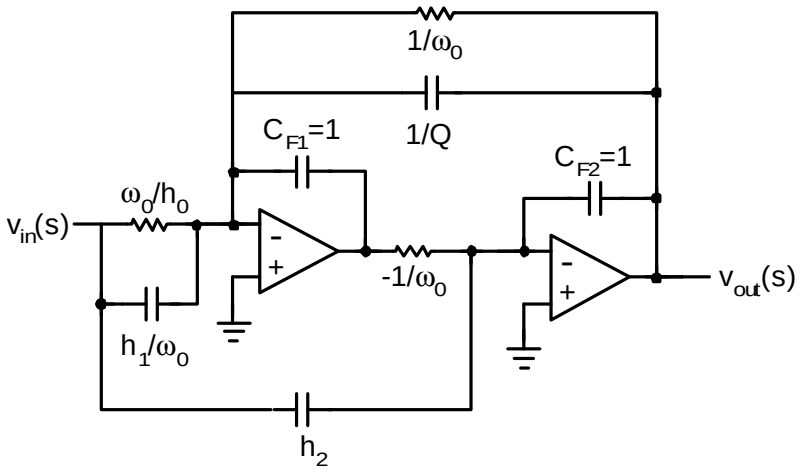
- **Transfer Function**

$$H(z) \equiv \frac{V_{out}(z)}{V_{in}(z)} = -\frac{(k_2+k_3)z^2+(k_1k_5-k_2-2k_3)z+k_3}{(1+k_6)z^2+(k_4k_5-k_6-2)z+1} = -\frac{a_2z^2+a_1z+a_0}{b_2z^2+b_1z+1}$$

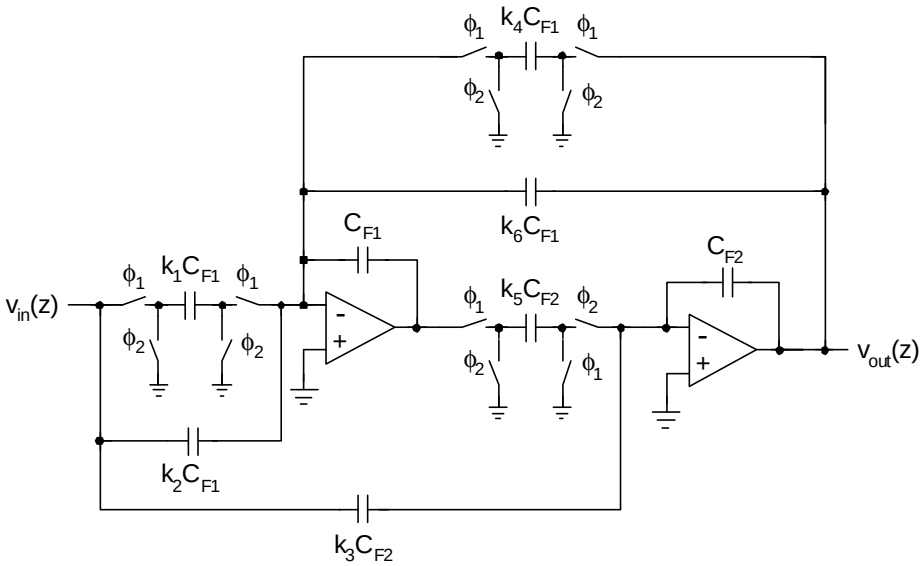
$$k_3 = a_0$$
$$k_2 = a_2 - a_0$$
$$k_1k_5 = a_0 + a_1 + a_2$$
$$k_6 = b_2 - 1$$
$$k_4k_5 = 1 + b_1 + b_2$$

High-Q SC Biquad

- **Active RC Version**



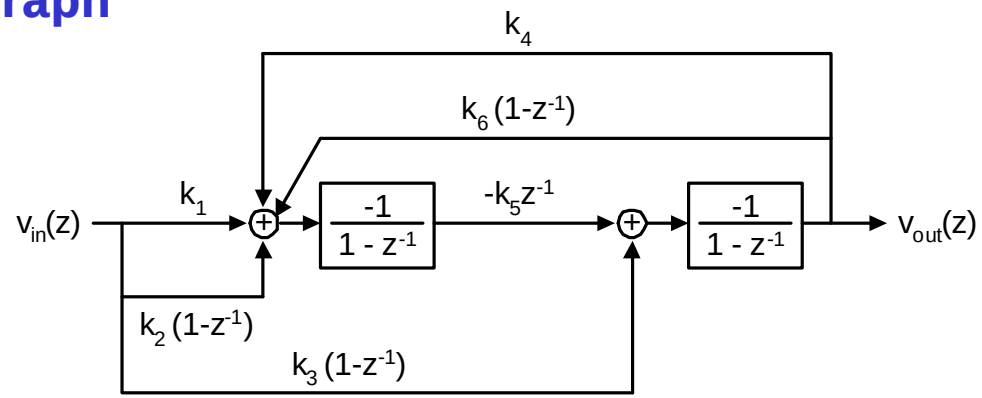
- **SC Version**



$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = -\frac{h_2 s^2 + h_1 s + h_0}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2}$$

High-Q SC Biquad (cont'd)

- **Signal Flow Graph**



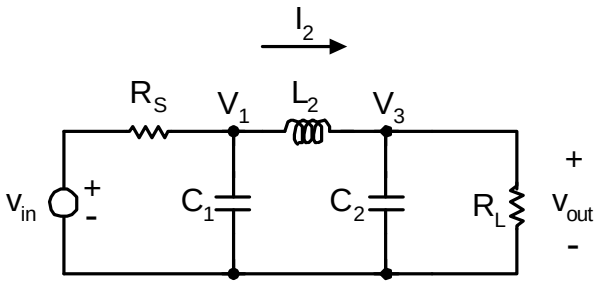
- **Transfer Function**

$$H(z) \equiv \frac{V_{out}(z)}{V_{in}(z)} = -\frac{k_3 z^2 + (k_1 k_5 + k_2 k_5 - 2k_3)z + (k_3 - k_2 k_5)}{z^2 + (k_4 k_5 + k_5 k_6 - 2)z + (1 - k_5 k_6)} = -\frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0}$$

$$k_3 = a_2$$
$$k_2 k_5 = a_2 - a_0$$
$$k_1 k_5 = a_0 + a_1 + a_2$$
$$k_5 k_6 = 1 - b_0$$
$$k_4 k_5 = 1 + b_1 + b_0$$

SC Ladder Filter

- **RLC Prototype**

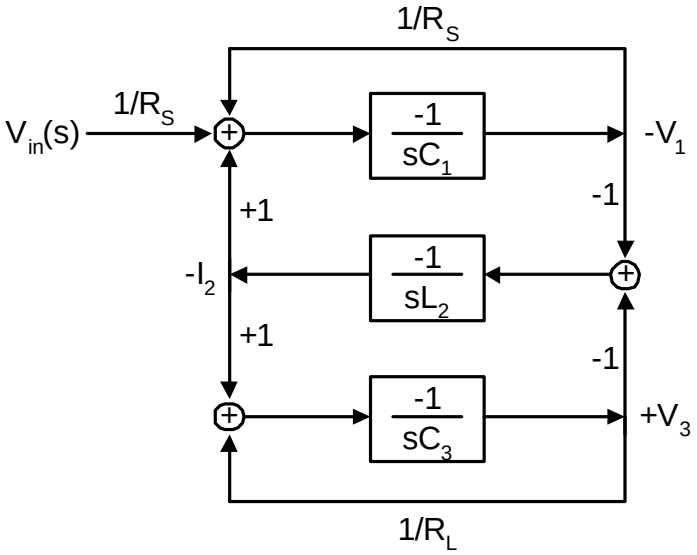


$$-V_1 = -\frac{1}{sC_1}\cdot\left[\frac{V_{in}+(-V_1)}{R_S}+(-I_2)\right]$$

$$-I_2 = -\frac{1}{sL_2}\cdot(V_1 - V_3)$$

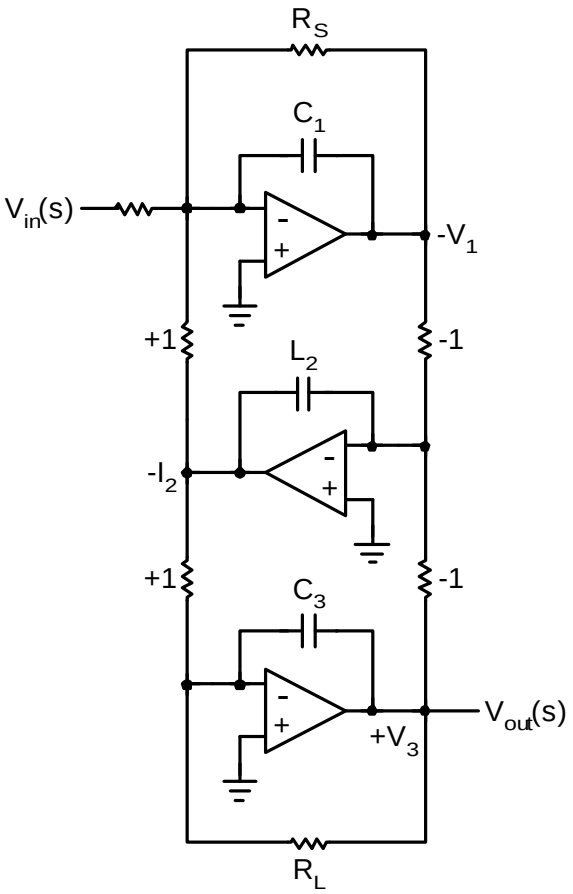
$$V_3 = -\frac{1}{sC_3}\cdot\left[(-I_2)+\frac{V_3}{R_L}\right]$$

- **CT Block Diagram**



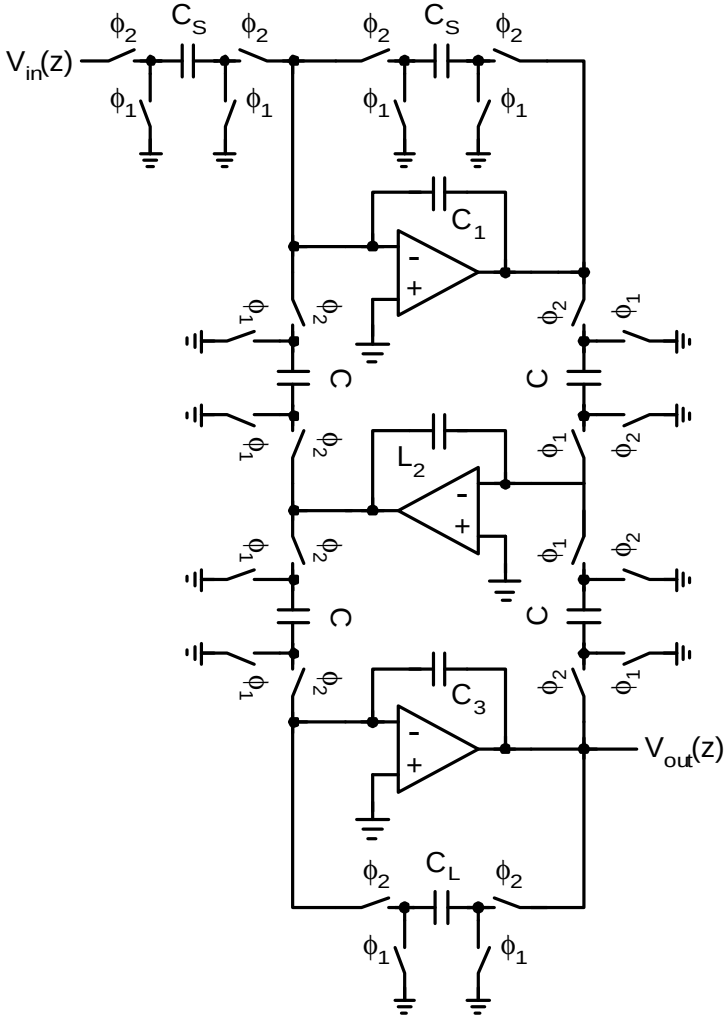
SC Ladder Filter (cont'd)

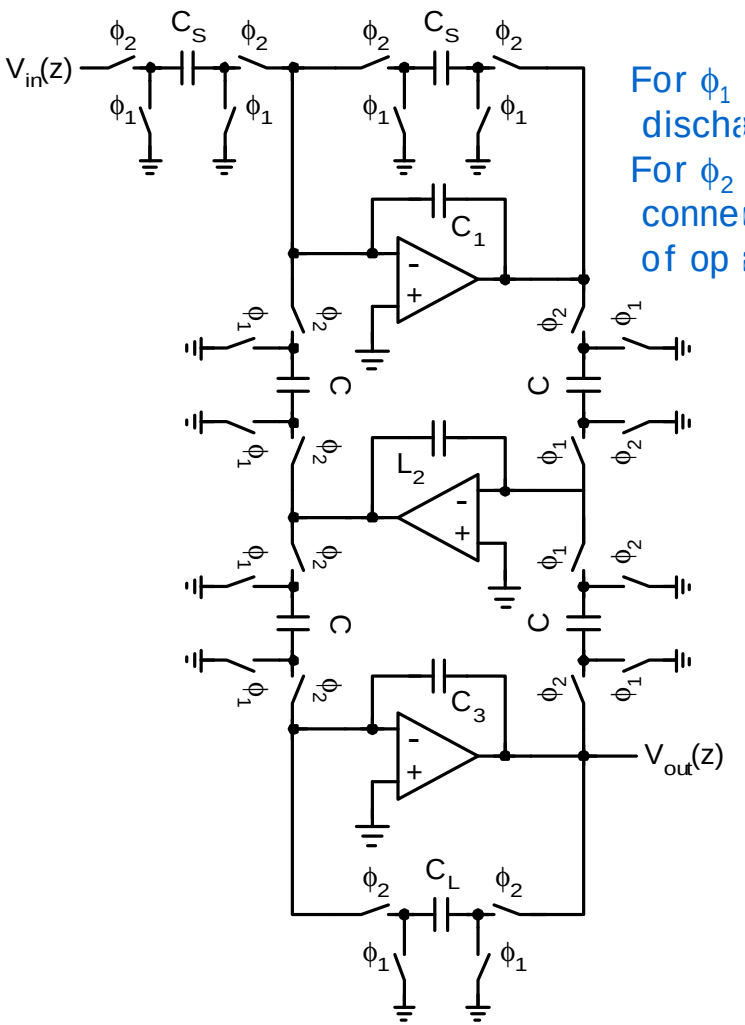
- **Active RC Implementation**



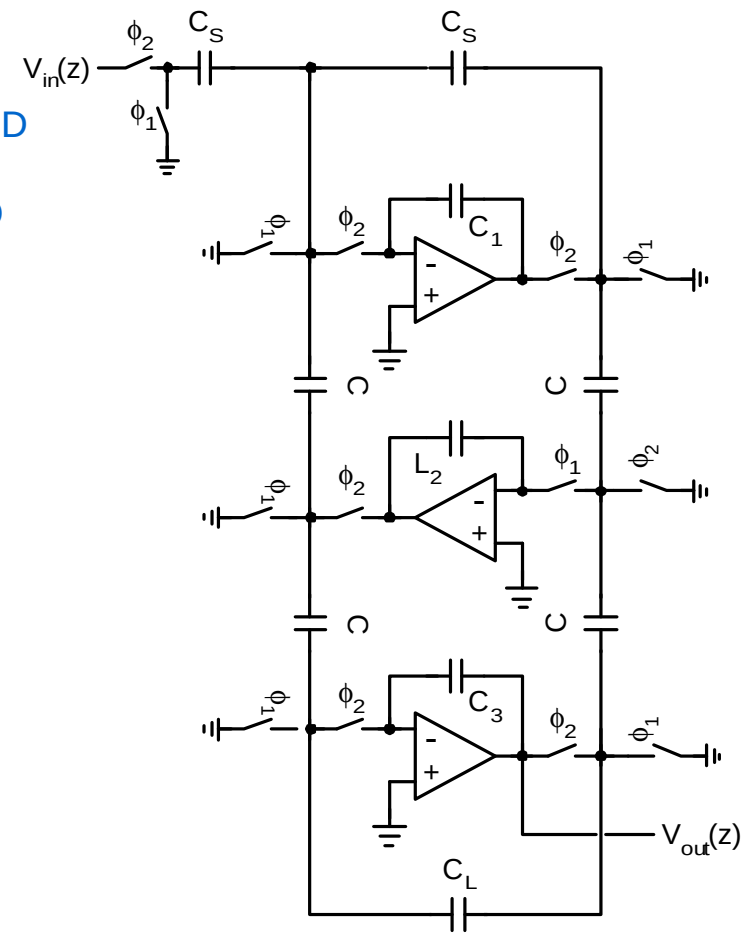
$$C_S \rightarrow T/R_S$$
$$C_L \rightarrow T/R_L$$
$$C \rightarrow T/1$$

- **SC Implementation**





For ϕ_1
discharged to GND
For ϕ_2
connected to I/O
of op amp.

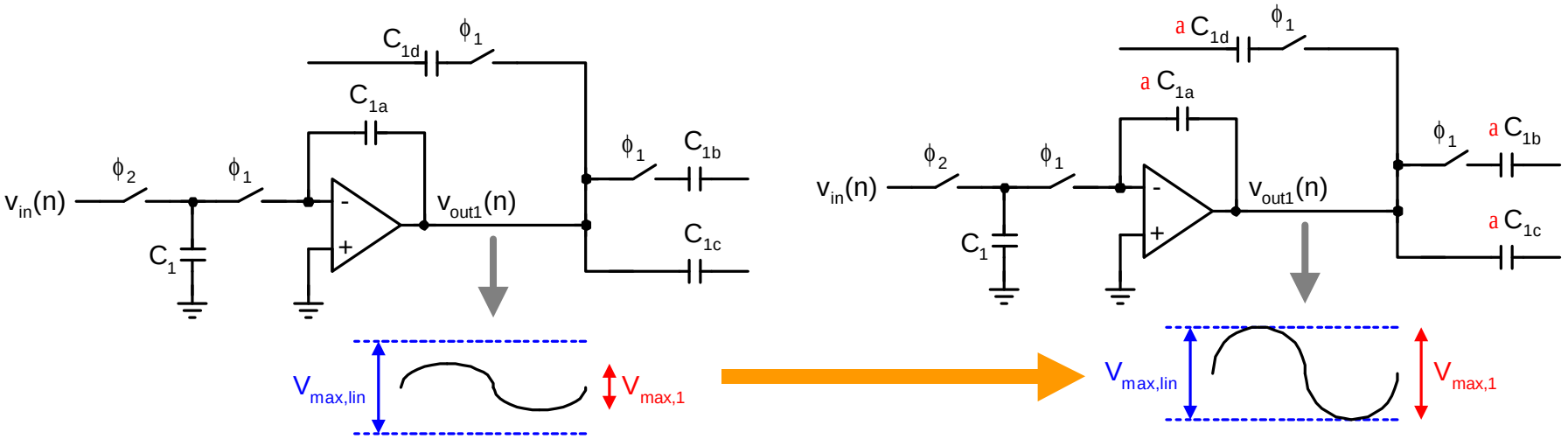


Scaling for Maximum Dynamic Range

- **Capacitors Connected to Output of Op Amp k, $C_{m,k}$**

$$C_{m,k} \bullet \alpha_k \rightarrow V_{out,k} / \alpha_k$$

- **For Maximum Output of Op Amp k, $V_{max,k}$ $a_k = V_{max,k} / V_{max,lin}$**



- **Noise Increase by Much Less than O(a_k)**

Scaling for Minimum Capacitance

- **Capacitors Connected to Input of Op Amp k, $C_{n,k}$**

$$C_{n,k} \bullet \beta_k \rightarrow V_{in,k}$$

- **For Minimum Capacitance of Op Amp k, $C_{min,k}$**

$$\beta_k = C_{min} / C_{min,k}$$

where C_{min} is the min. capacitance value set by technology.

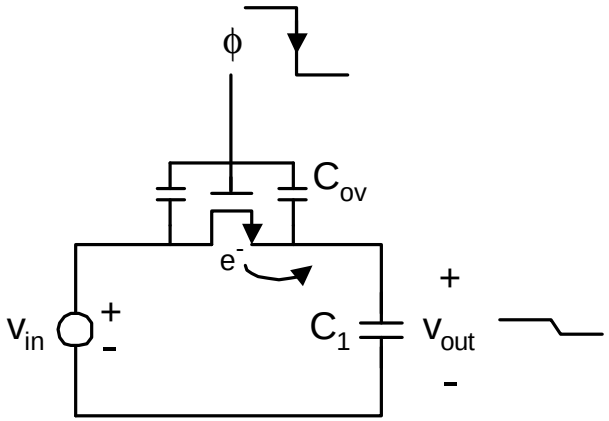
- **Smallest Capacitor Connected to Input of Op Amp k ~ C_{min}**

- **Total Capacitance Minimized**

Non-ideal Problems in SC FIlters

- **Switch Nonidealities**
  - ✓ Non-Zero On-Resistance
  - ✓ Charge Injection
  - ✓ Junction Leakage Current
- **Capacitance Nonidealities**
  - ✓ Mismatch Problem
- **Op Amp Nonidealities**
  - ✓ Offset Voltage
  - ✓ Finite DC Gain & Bandwidth
  - ✓ Limited Slew Rate
  - ✓ Non-Zero Output Impedance
  - ✓ Noise

Charge Injection



- **Due to Overlap Capacitance C_{OV} ➔ Signal Independent**

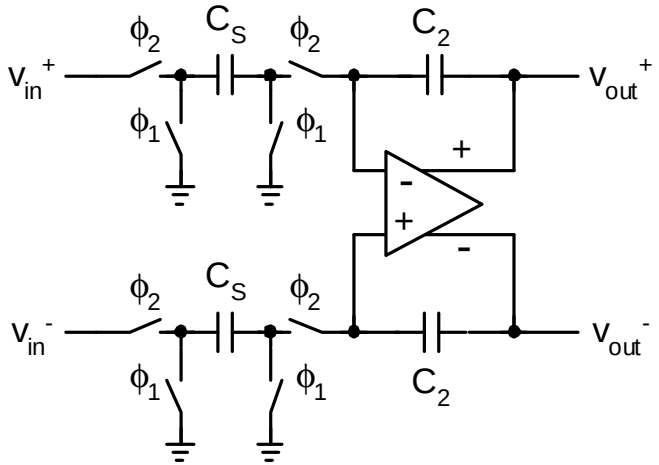
$$\Delta V_{OV} = -\frac{C_{OV}}{C_1 + C_{OV}} \cdot (V_{DD} - V_{SS})$$

- **Due to Channel Charge ΔQ_{CH} ➔ Signal Dependent**

$$\Delta V_{CH} = \frac{\Delta Q_{CH}/2}{C_1} = -\frac{C_{ox} WL (V_{GS} - V_{TH})}{2C_1} = -\frac{C_{ox} WL (V_{DD} - V_S - V_{TH})}{2C_1}$$

Solution - DV_{OV}

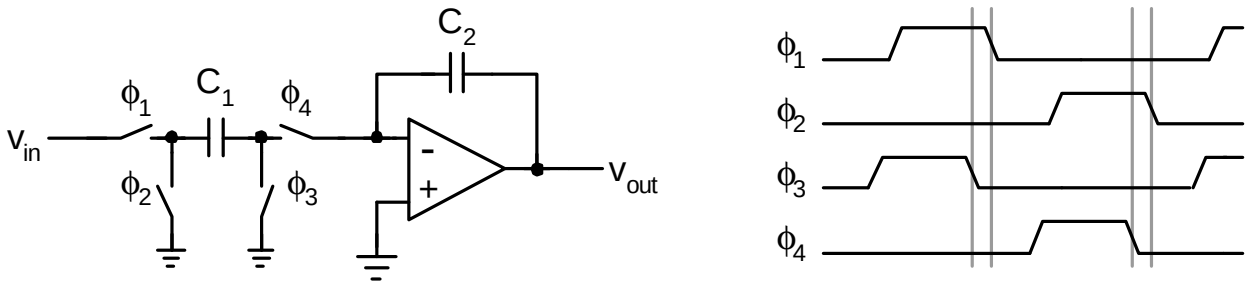
- **Half-Size Dummy Switch Driven By Complement Clocks**
- **Transmission Gate**
- **Fully Differential Approach**



➔ $\Delta V_{ov}^{(+)}$ & $\Delta V_{ov}^{(-)}$ Cancelled Each Other

Solution - DV_{CH}

- **Delayed Clocking Scheme**



✓ Due to S_1 : Channel Charge Dependent on V_{in}

✓ Due to S3 & S4 : Channel Charge Dependent on GND

➔ Can be Removed

✓ Turing Off S_3 & S_4 Earlier ➔ Channel Charge of S_1 Isolated from C_2

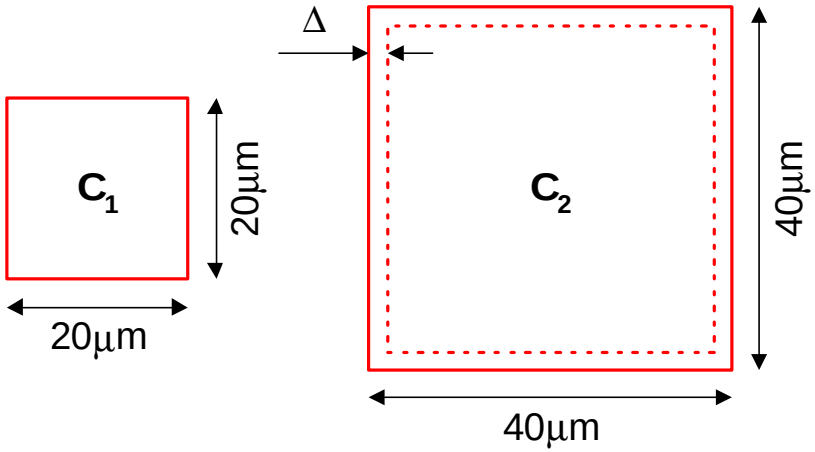
- **Using Compensation Capacitor**

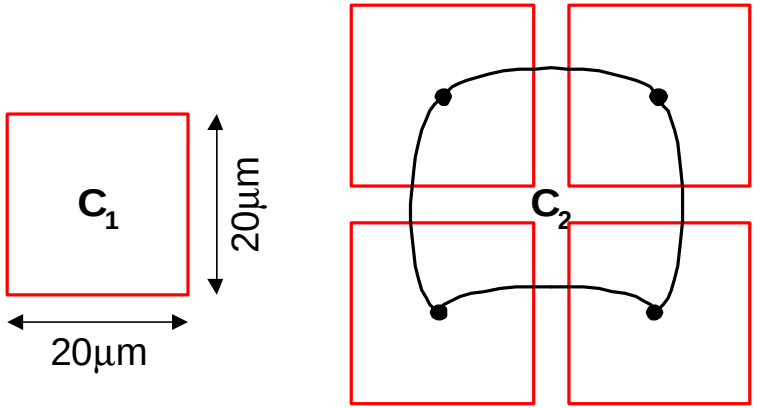
➔ Insert $(-)\Delta Q_{CH}$ Stored on Compensation Capacitor

Capacitance Mismatch

- **Area Inaccuracy & Oxide Thickness Variation**

- **Keep Capacitance Ratio Constant**





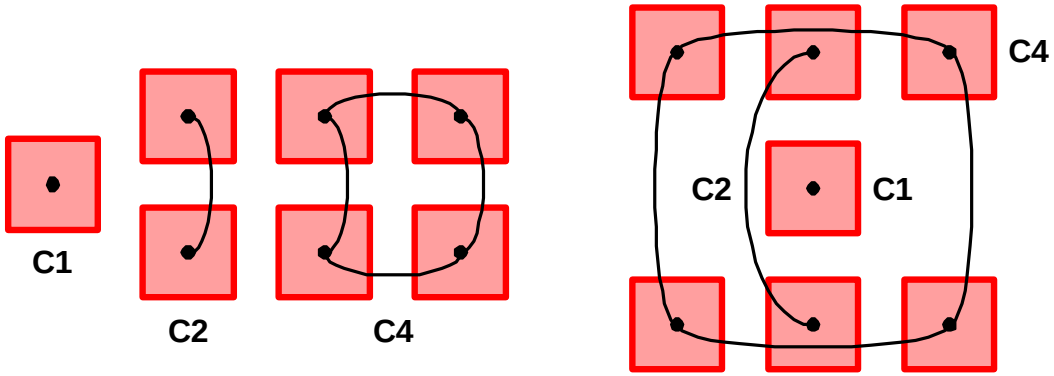
$$\frac{C_2}{C_1} = \frac{(40-0.5)\cdot(40-0.5)}{(20-0.5)\cdot(20-0.5)} = 4.103$$

← 2.6% error

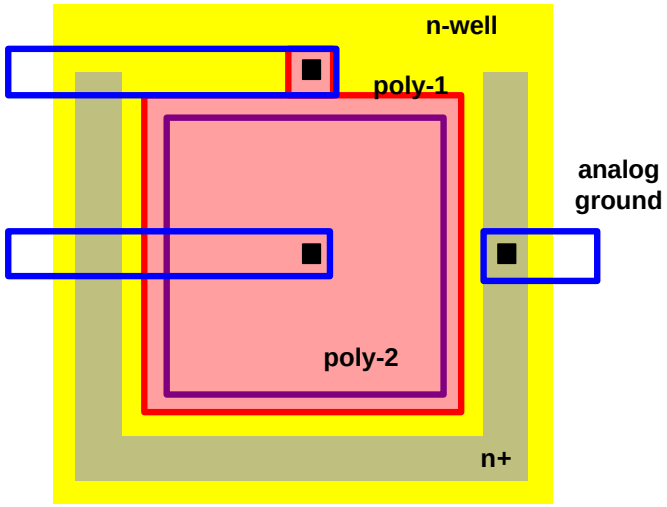
$$\frac{C_2}{C_1} = \frac{4(20-0.5)\cdot(20-0.5)}{(20-0.5)\cdot(20-0.5)} = 4$$

Capacitance Layout

- **Commom-Centroid Approach**



- **Ground Shielding**

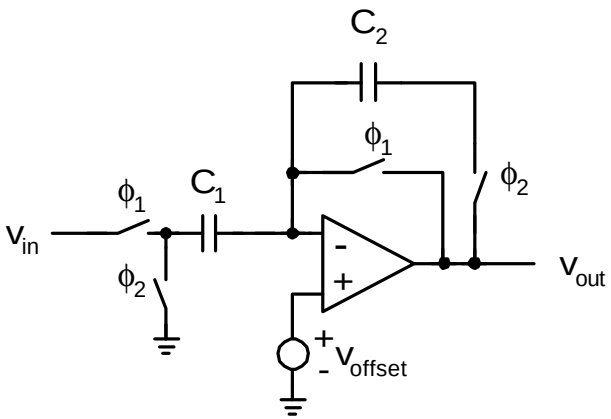


CDS Technique

- **Correlated Double Sampling**

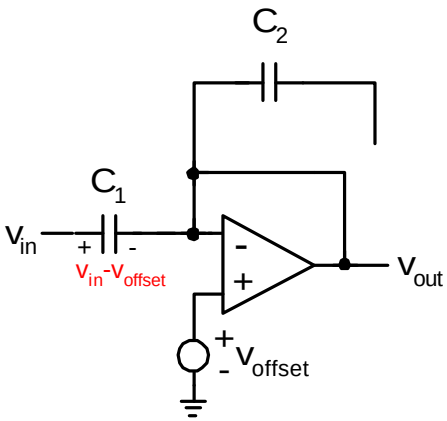
- **Can Remove**

  Offset Voltage, 1/f-Noise, Power Supply Noise, Finite DC Gain Error



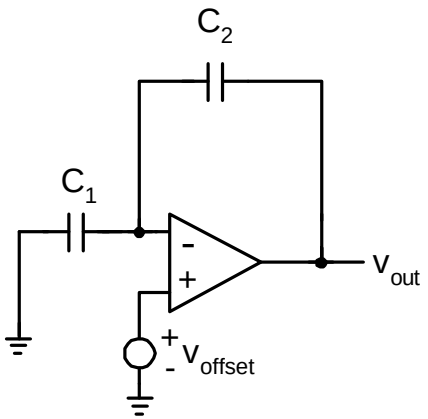
- f_1

V_{offset} Stored

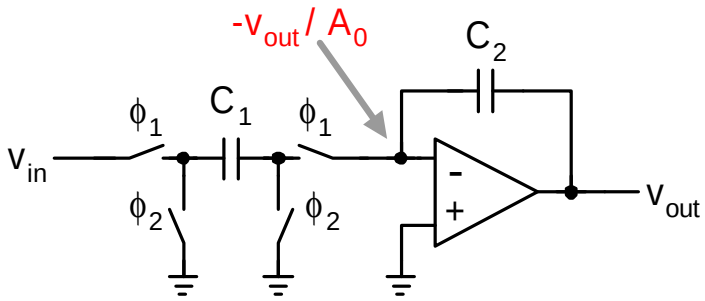


- f_2

V_{offset} Removed



Finite DC Gain of Op Amp



- **Transfer Function**

$$H(z) = -\frac{C_1/C_2}{\left(1+\frac{1+C_1/C_2}{A_0}\right)-\left(1+\frac{1}{A_0}\right)z^{-1}}$$

- **Frequency Response**

$$H\left(e^{j\omega T}\right) = \frac{H_{ideal}\left(e^{j\omega T}\right)}{1-m(\omega)-j\theta(\omega)} = -\frac{C_1}{C_2}\cdot\frac{e^{j\omega T/2}}{j\sin(\omega T/2)}\cdot\frac{1}{1-m(\omega)-j\theta(\omega)}$$

- **Magnitude Error**

$$m(\omega) = -\frac{1+C_1/2C_2}{A_0}$$

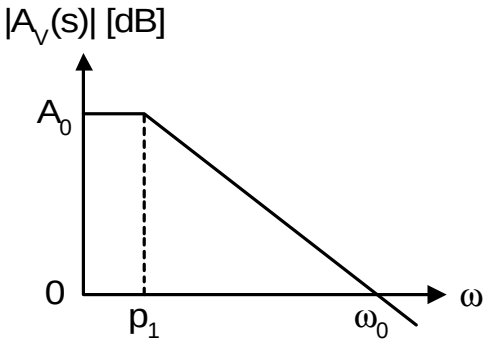
- **Phase Error**

$$\theta(\omega) = \frac{C_1/C_2}{2A_0\sin(\omega T/2)}$$

Finite Bandwidth of Op Amp

- **Op Amp : One-Pole System w/ Unity Gain Freq. of w_0**

$$A_V(s) = \frac{A_0}{1 + s/p_1} = \frac{A_0 \cdot p_1}{s + p_1} = \frac{\omega_0}{s + p_1}$$



- **Frequency Response**

$$H\left(e^{j\omega T}\right) = F(\omega) \cdot H_{ideal}\left(e^{j\omega T}\right) = -\frac{C_1}{C_2} \cdot \frac{e^{j\omega T/2}}{j\sin(\omega T/2)} \cdot F(\omega)$$

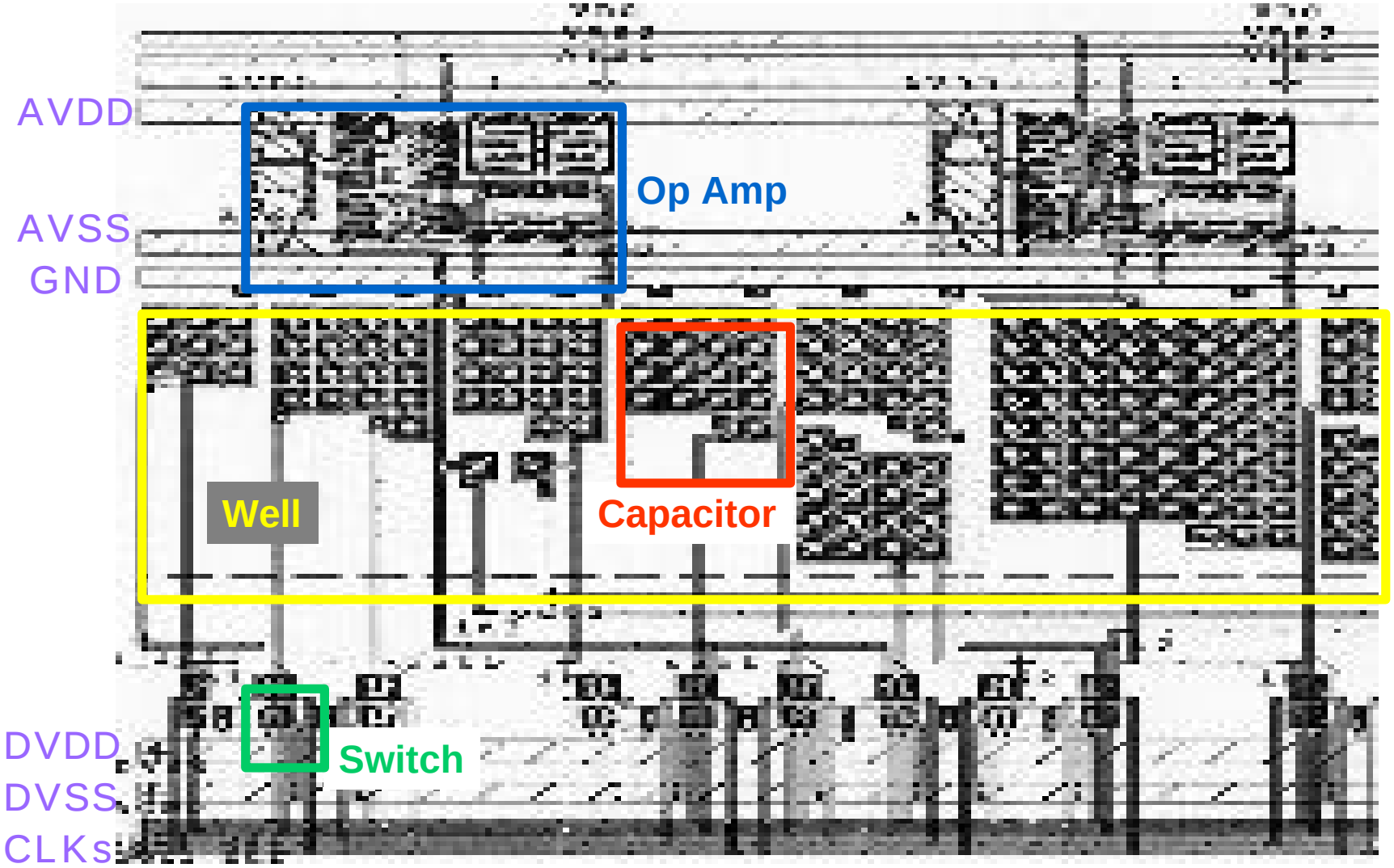
- **Magnitude Error**

$$|F(\omega)| = 1 + m(\omega) = 1 - e^{-\frac{C_2}{C_1+C_2}\frac{\omega_0 T}{2}} 1 - \frac{C_2}{C_1 + C_2}\cos(\omega_o T)$$

- **Phase Error**

$$\angle F(\omega) = \theta(\omega) = -e^{-\frac{C_2}{C_1+C_2}\omega_0 T/2} \cdot \frac{C_1}{C_1 + C_2}\sin(\omega_0 T)$$

Layout Example



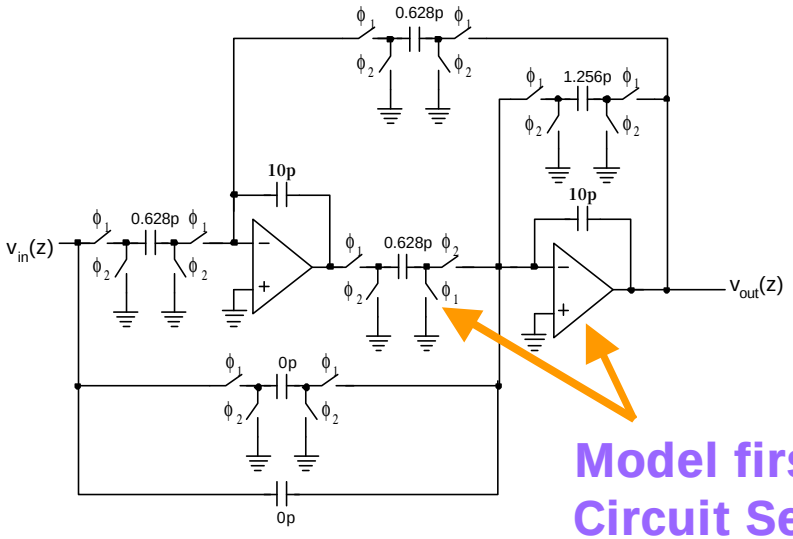
SC Filter Simulation Example

■ **Low-Q SC Lowpass Biquad Filter**

FFT Analysis for Each Frequency of Interest

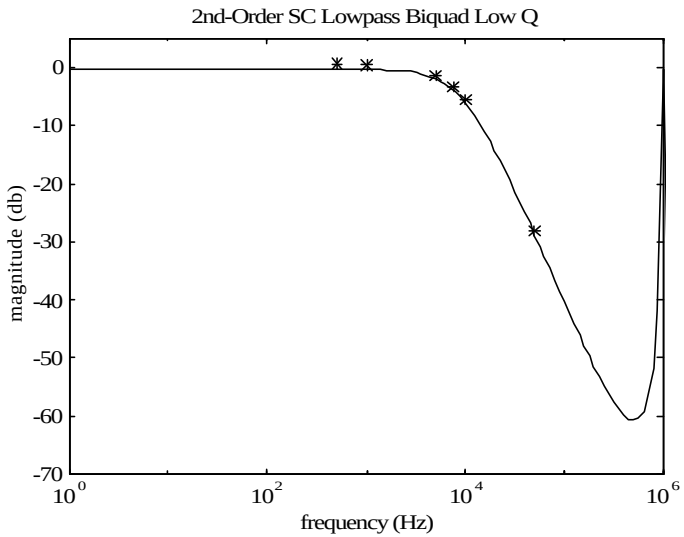
.fft v(node) np = 2048 format = unorm

● **Circuit Schematic**



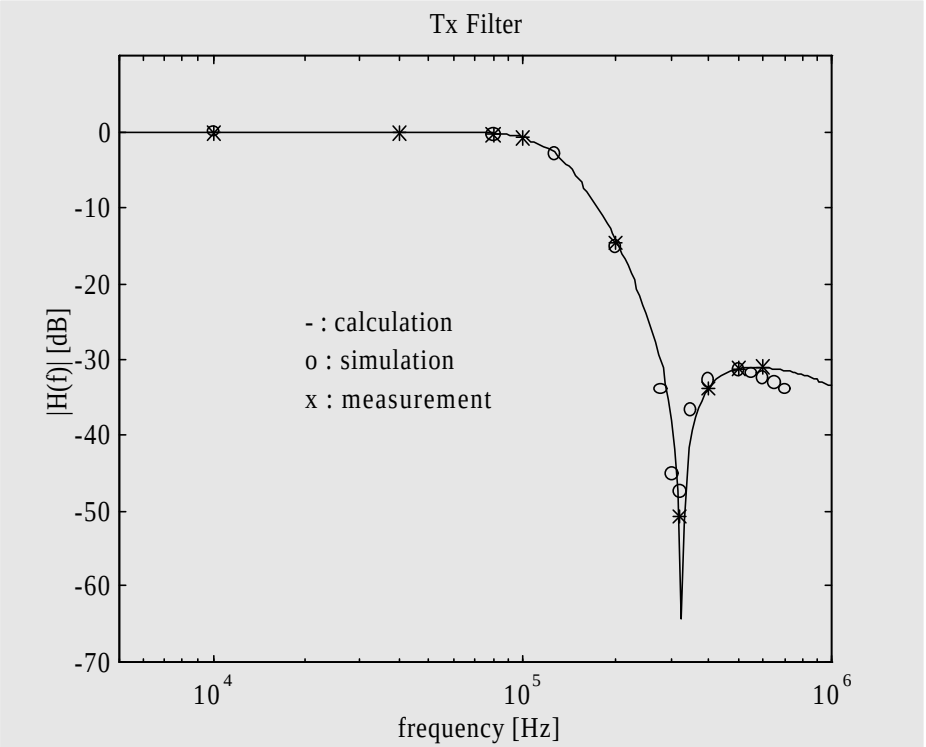
Model first
Circuit Second

● **Simulation Results**



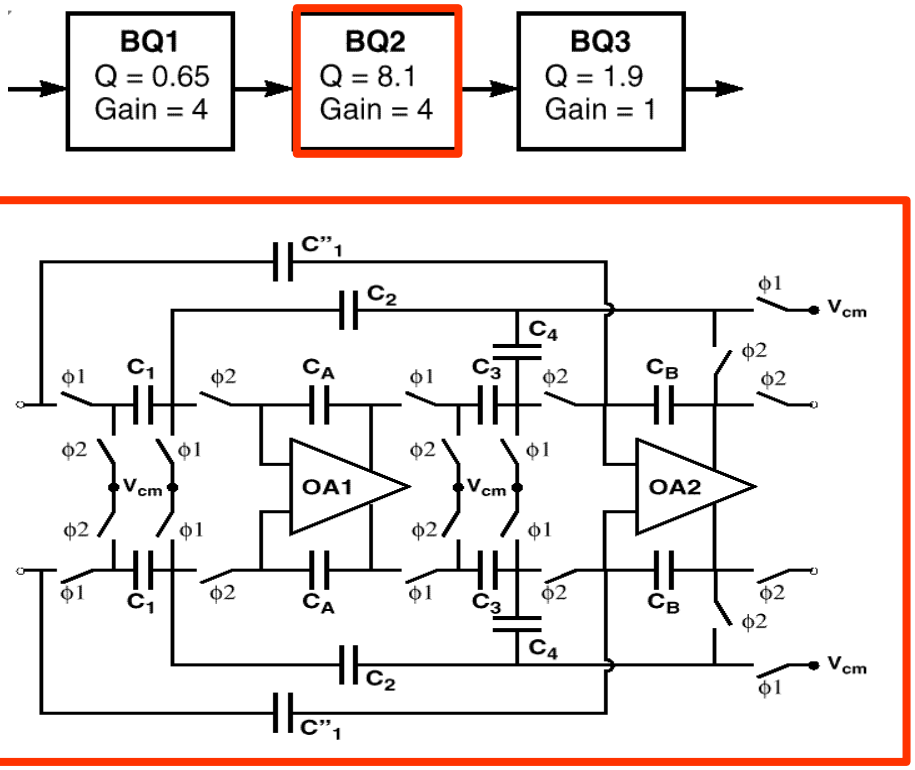
Implementation Example

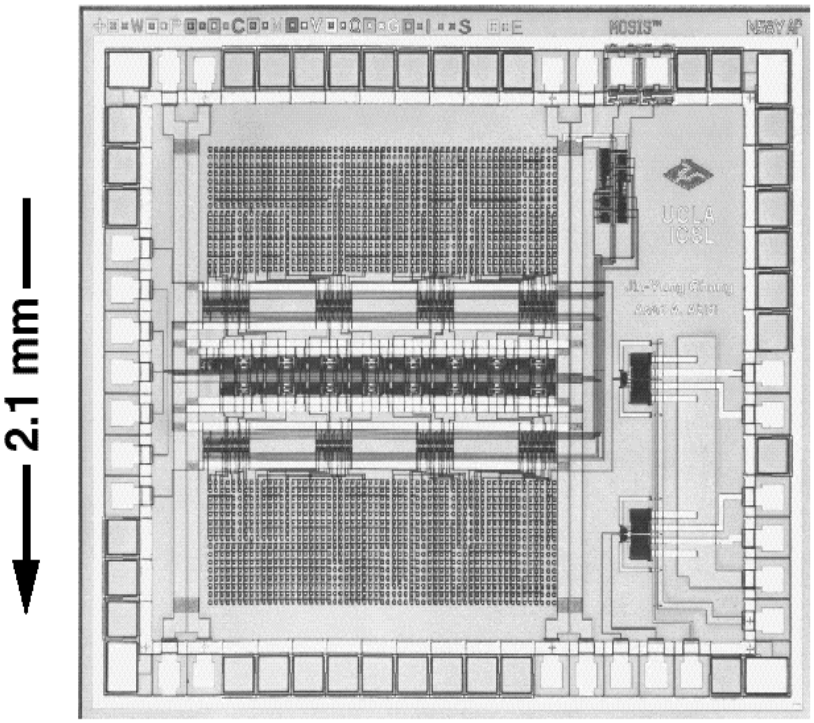
5th-Order Lowpass Filter for ISDN U-I/F AFE



Recent Advance Example 1

6th-Order Channel Select Lowpass Filter

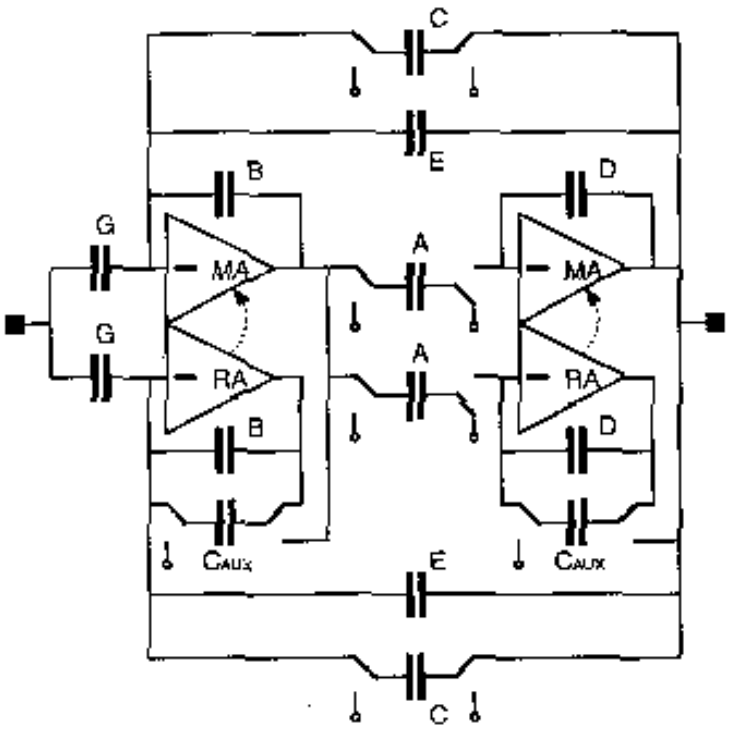




📖 *IEEE VLSI Symposium* 1996.

Recent Advance Example 2

Bandpass Biquad w/ Gain-Enhancement Replica Op Amp



A=C=1 B=D=1.613 G=E=0.1613 (T-network)

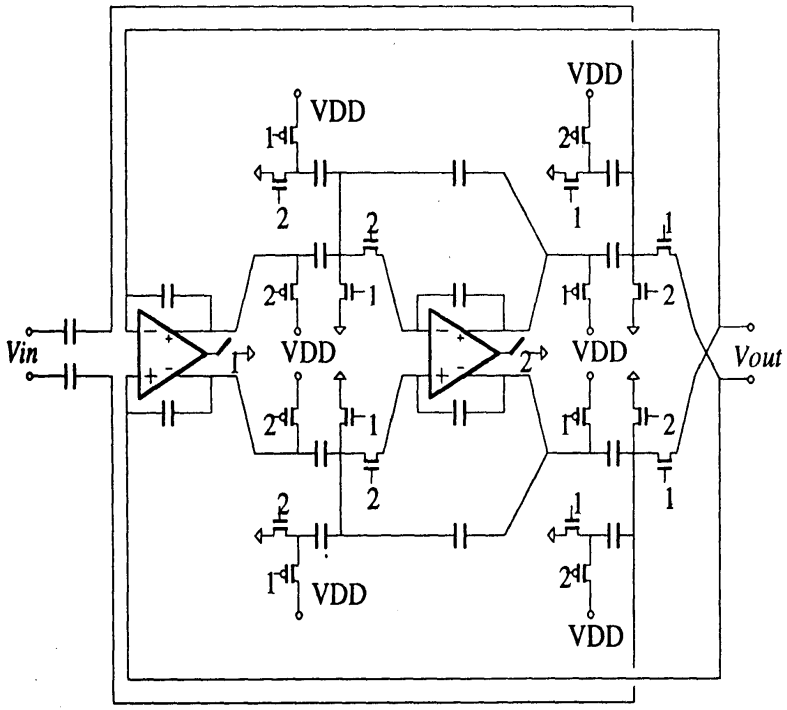
f_{center} = 10MHz (Q=10)

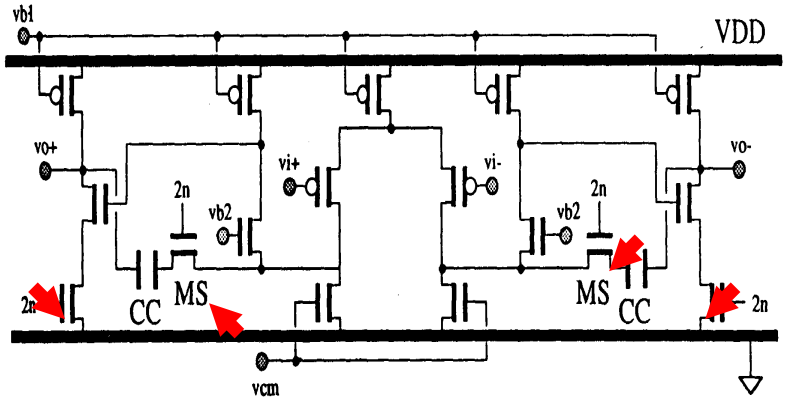
f_{sample} = 100MHz

📖 *IEEE ISSCC* 1997.

Recent Advance Example 3

Bandpass Biquad w/ Switched Op Amp





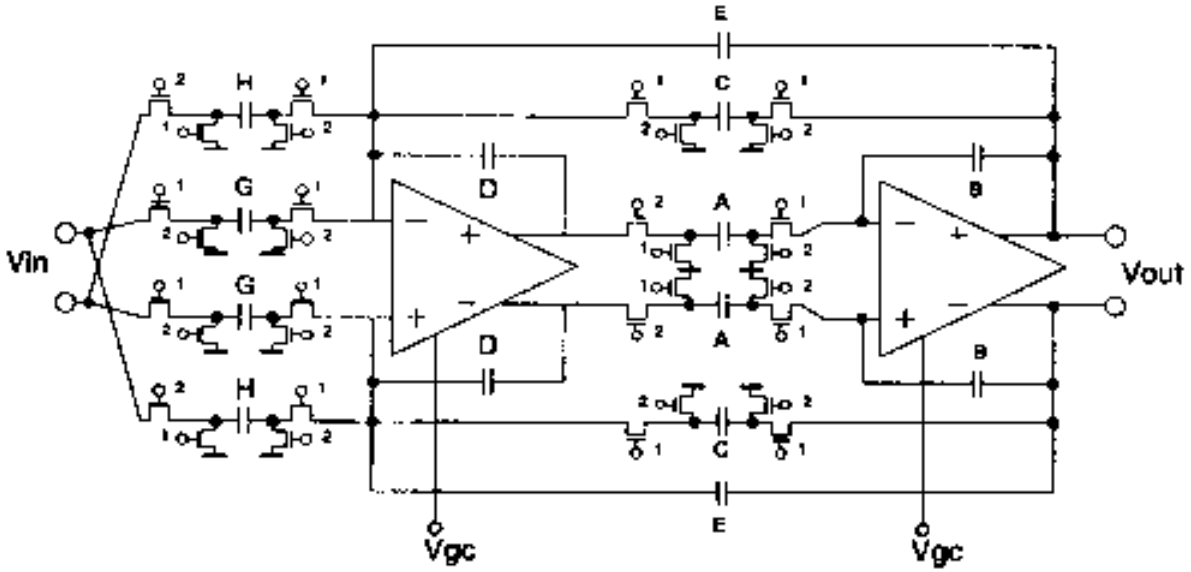
f_{center} = 440kHz (Q=6.7) w/ f_s = 1.8MHz

Power = 160μW @ V_{DD}=1V

📖 *IEEE ISSCC* 1997.

Recent Advance Example 4

200MSampes/s SC-LPF



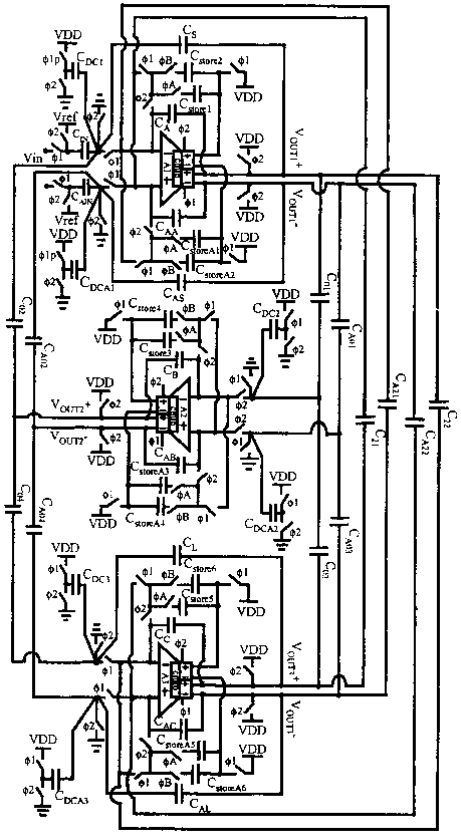
0.5-μm CMOS Technology

Power = 10mW @ V_{DD}=3V

📖 *IEEE ISSCC* 1999.

Recent Advance Example 5

1V SC-BPF w/ Switched Op Amp



0.5-μm CMOS Technology

f_o = 75kHz w/ Q = 45

Power = 310μW @ V_{DD}=1V

📖 *IEEE ISSCC* 2000.